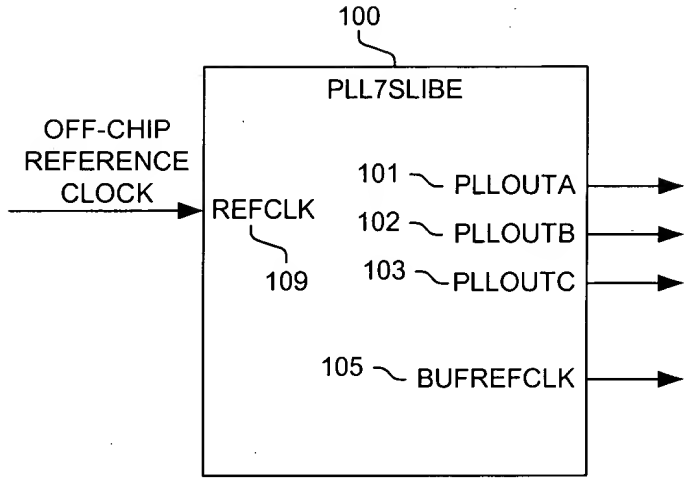
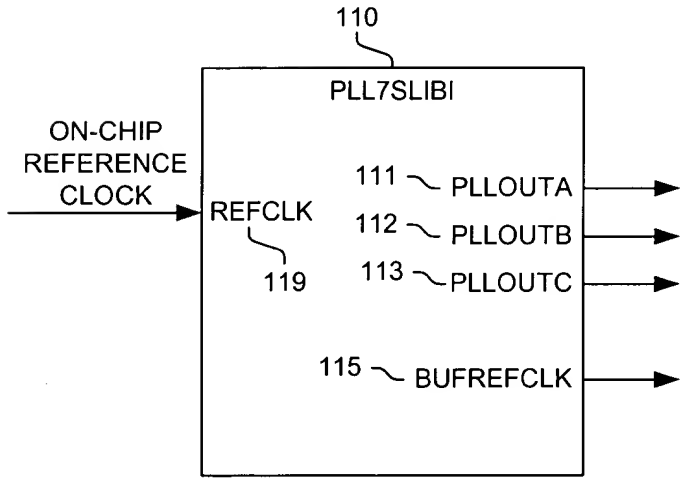
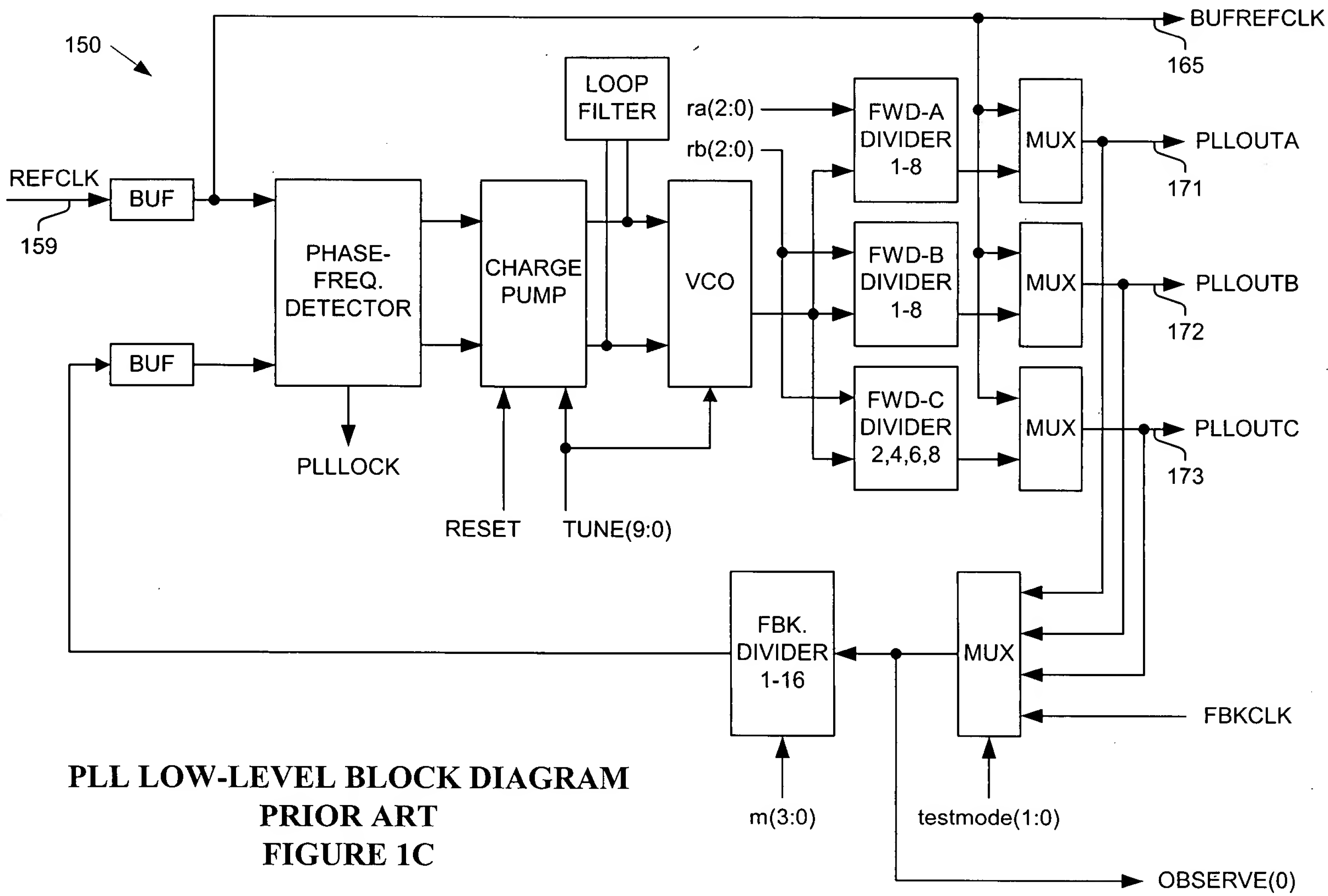


PLL7SLIBE
PRIOR ART
FIGURE 1A



PLL7SLIBI
PRIOR ART
FIGURE 1B



PLL LOW-LEVEL BLOCK DIAGRAM
PRIOR ART
FIGURE 1C

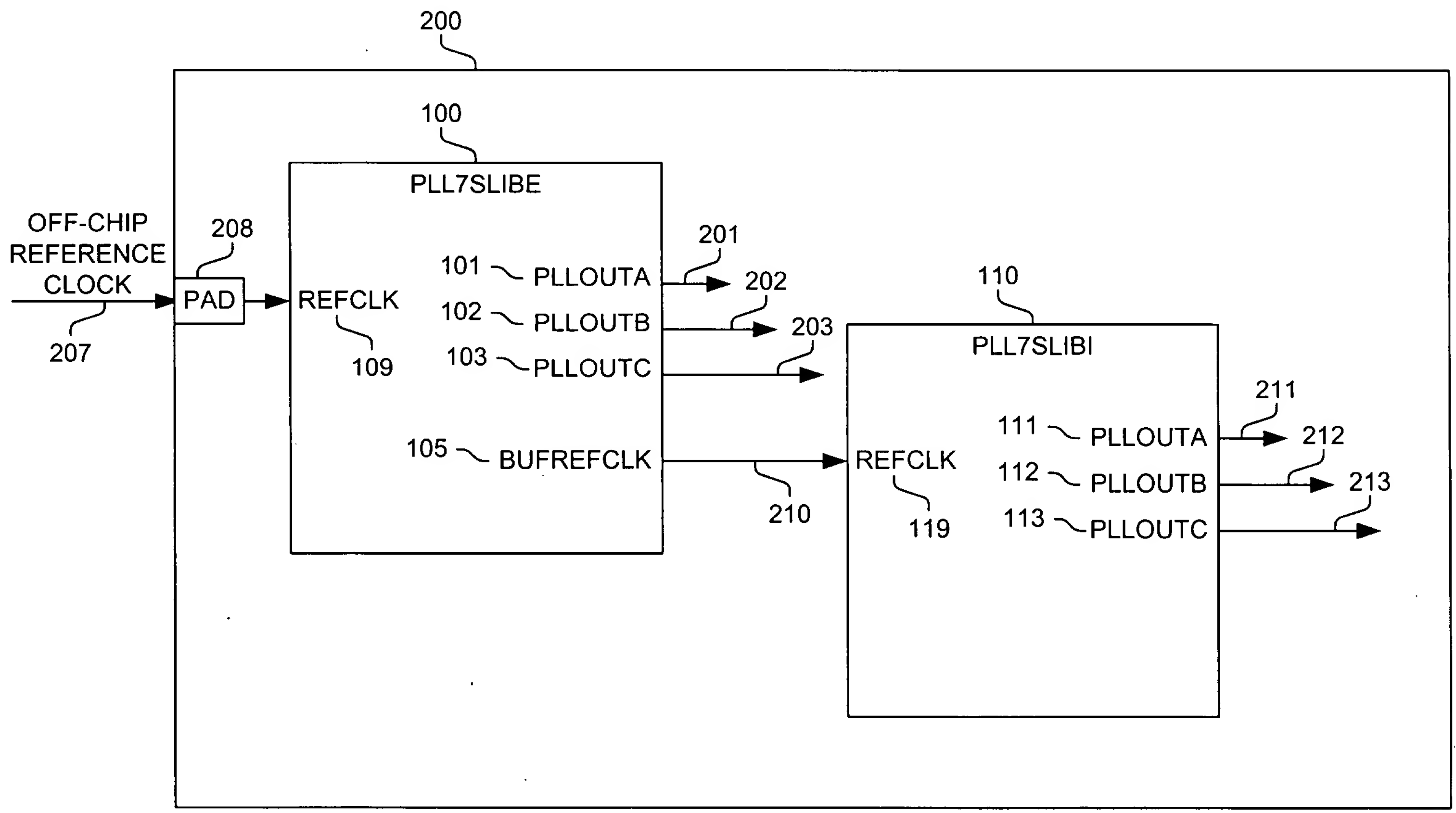

200
100
PLL7SLIBE
OFF-CHIP
REFERENCE
CLOCK
208
PAD
207
REFCLK
109
101
PLLOUTA
102
PLLOUTB
103
PLLOUTC
105
BUFREFCLK
201
202
203
210
110
PLL7SLIBI
REFCLK
119
111
PLLOUTA
112
PLLOUTB
113
PLLOUTC
211
212
213

FIGURE 2

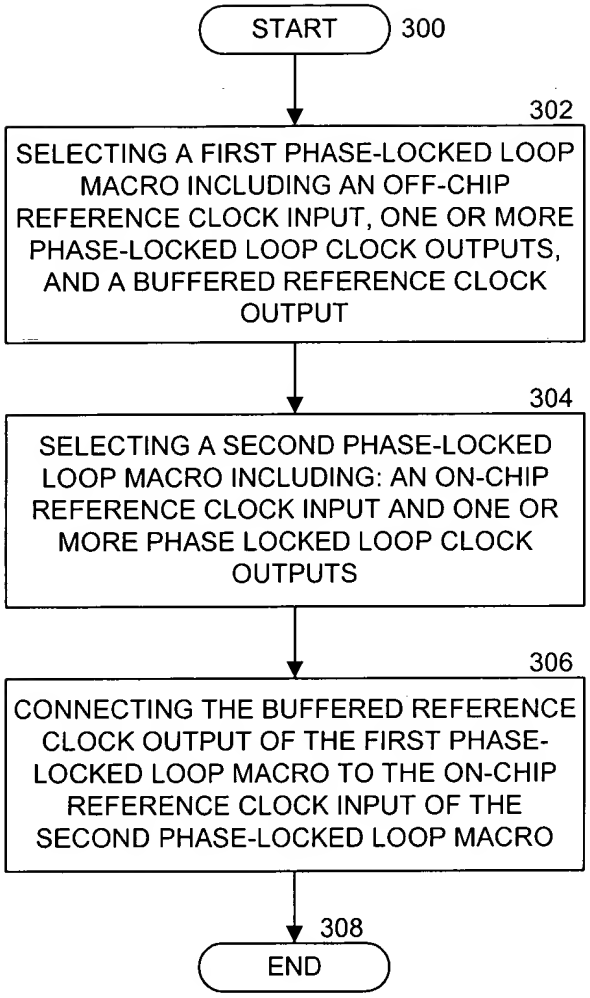

START
300
302
SELECTING A FIRST PHASE-LOCKED LOOP MACRO INCLUDING AN OFF-CHIP REFERENCE CLOCK INPUT, ONE OR MORE PHASE-LOCKED LOOP CLOCK OUTPUTS, AND A BUFFERED REFERENCE CLOCK OUTPUT
304
SELECTING A SECOND PHASE-LOCKED LOOP MACRO INCLUDING: AN ON-CHIP REFERENCE CLOCK INPUT AND ONE OR MORE PHASE LOCKED LOOP CLOCK OUTPUTS
306
CONNECTING THE BUFFERED REFERENCE CLOCK OUTPUT OF THE FIRST PHASE-LOCKED LOOP MACRO TO THE ON-CHIP REFERENCE CLOCK INPUT OF THE SECOND PHASE-LOCKED LOOP MACRO
308
END

FIGURE 3A

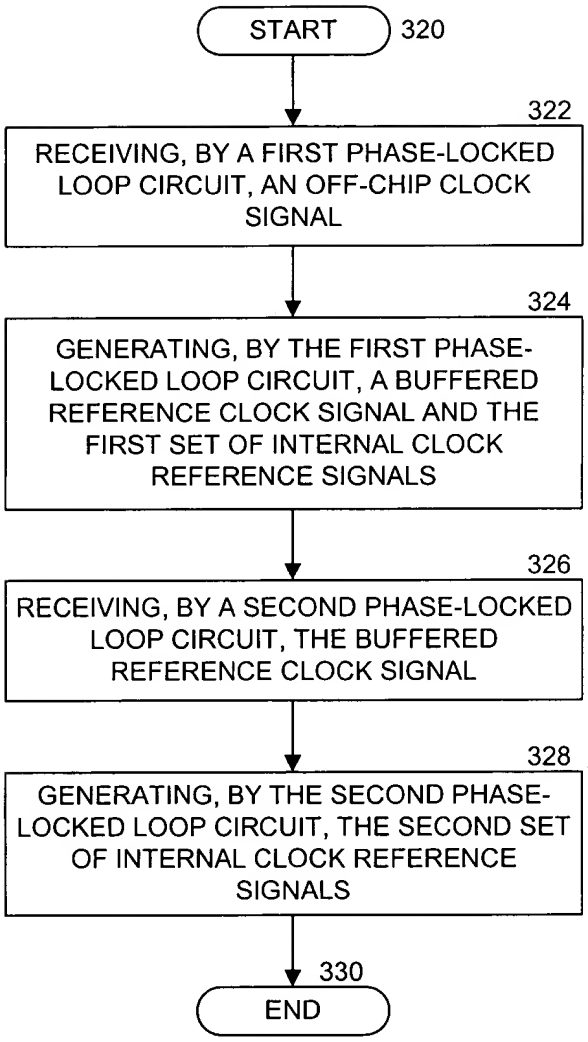

START
320
322
RECEIVING, BY A FIRST PHASE-LOCKED LOOP CIRCUIT, AN OFF-CHIP CLOCK SIGNAL
324
GENERATING, BY THE FIRST PHASE-LOCKED LOOP CIRCUIT, A BUFFERED REFERENCE CLOCK SIGNAL AND THE FIRST SET OF INTERNAL CLOCK REFERENCE SIGNALS
326
RECEIVING, BY A SECOND PHASE-LOCKED LOOP CIRCUIT, THE BUFFERED REFERENCE CLOCK SIGNAL
328
GENERATING, BY THE SECOND PHASE-LOCKED LOOP CIRCUIT, THE SECOND SET OF INTERNAL CLOCK REFERENCE SIGNALS
330
END

FIGURE 3B